



KINGS

COLLEGE OF ENGINEERING



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

Subject Code: EC1206

Year/Sem: II/III

Subject Name: DIGITAL PRINCIPLES AND SYSTEMS DESIGN

Unit – I BOOLEAN ALGEBRA AND LOGIC GATES PART-A (2 Marks)

1. Define binary logic.
2. State the different classification of binary codes.
3. State the steps involved in Gray to binary conversion.
4. What is meant by bit & byte?
5. What is the use of Don't care conditions?
6. List different number systems.
7. State the abbreviations of ASCII and EBCDIC code
8. What are the different types of number complements?
9. State De Morgan's theorem.

PART-B

1. Simplify the following Boolean function by using Tabulation method $F(w, x, y, z) = \Sigma(0,1,2,8,10,11,14,15)$ (16)
2. Simplify the following Boolean functions by using K'Map in SOP & POS.
 $F(w, x, y, z) = \Sigma(1,3,4,6,9,11,12,14)$ (16)
3. Simplify the following Boolean functions by using K'Map in SOP & POS.
 $F(w, x, y, z) = \Sigma(1,3,7,11,15) + d(0,2,5)$ (16)
4. Reduce the given expression.
 $[(AB)' + A' + AB']$ (16)
5. Reduce the following function using k-map technique
 $f(A,B,C,D) = \pi M(0,3,4,7,8,10,12,14) + d(2,6)$ (16)

Unit – II
COMBINATIONAL LOGIC
PART-A (2 Marks)

1. What are Logic gates?
2. What are the basic digital logic gates?
3. What is BCD adder?
4. What is Magnitude Comparator?
5. What is code conversion?
6. Draw the logic circuit of full adder using half adder
7. What is code converter?
8. Define Combinational circuit.
9. Define sequential circuits.
10. What is Binary parallel adder?

PART-B

1. Design a combinational logic circuit to convert the Gray code into Binary code. (16)
2. Draw the truth table and logic diagram for full-Adder. (16)
3. Draw the truth table and logic diagram for full-Subtractor. (16)
4. Explain Binary parallel adder. (16)
5. Design a combinational logic circuit to convert the BCD to Binary code. (16)

Unit III
DESIGN WITH MSI DEVICES
PART-A (2 Marks)

1. Define Multiplexing?
2. What is Demultiplexer?
3. Define decoder & binary decoder
4. Define Encoder & priority Encoder
5. Give the applications of Demultiplexer.
6. Mention the uses of Demultiplexer.
7. List the types of ROM.
8. Differentiate ROM & PLD's
9. What are the different types of RAM?
10. What are the types of arrays in RAM?

PART-B

1. Implement the following function using PLA. (16)
 - $A(x, y, z) = \Sigma m(1, 2, 4, 6)$
 - $B(x, y, z) = \Sigma m(0, 1, 6, 7)$
 - $C(x, y, z) = \Sigma m(2, 6)$
2. Implement the following function using PAL. (16)
 - $W(A, B, C, D) = \Sigma m(2, 12, 13)$
 - $X(A, B, C, D) = \Sigma m(7, 8, 9, 10, 11, 12, 13, 14, 15)$
 - $Y(A, B, C, D) = \Sigma m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$
 - $Z(A, B, C, D) = \Sigma m(1, 2, 8, 12, 13)$
3. Implement the given function using multiplexer. (16)
4. Explain about Encoder and Decoder. (16)
5. Explain about 4 bit Magnitude comparator. (16)

Unit IV**SYNCHRONOUS SEQUENTIAL LOGIC****PART-A (2 Marks)**

1. What is sequential circuit?
2. List out the classifications of sequential circuit.
3. What is Synchronous sequential circuit?
4. List different types of flip-flops.
5. What do you mean by triggering of flip-flop?
6. What is an excitation table?
7. Give the excitation table of a JK flip-flop .
8. Give the excitation table of a SR flip-flop
9. Give the excitation table of a T flip-flop

PART-B

1. Design a counter with the following repeated binary sequence:0, 1, 2,3, 4, 5, 6.
use JK Flip-flop. (16)
2. Describe the operation of SR flip-flop . (16)
3. Design a sequential circuit using JK flip-flop for the following state table [use state diagram]

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
00	00	11	1	0
01	01	11	1	1
10	01	00	1	0
11	11	10	0	0

(16)

4. The count has a repeated sequence of six states, with flip flops B and C repeating the binary count 00, 01, 10 while flip flop A alternates between 0 and 1 every three counts. Design with JK flip-flop. (16)

5. Design a 3-bit T flip-flop counter. (16)

Unit V

ASYNCHRONOUS SEQUENTIAL LOGIC

PART-A (2 Marks)

1. What is the use of state diagram?
2. What is state table?
3. What is a state equation?
4. Differentiate ASM chart and conventional flow chart?
5. What is flow table?
6. What is primitive flow table?
7. Define race condition.
8. Define critical & non-critical race with example.
9. How can a race be avoided?
10. Define hazards.

PART-B

1. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input. (16)
2. Give hazard free relation for the following Boolean function.

- $F(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 10, 12)$ (16)
3. Explain about Hazards. (16)
4. Explain about Races? (16)
5. Design T Flip flop from Asynchronous Sequential circuit. (16)

Kings College of Engineering

Filename: DPSD QB1.doc
Directory: \\172.16.3.10\ece common\YR\QB-DPSD & POC
Template: C:\Documents and Settings\Administrator\Application
Data\Microsoft\Templates\Normal.dot
Title: KINGS
Subject:
Author: ECEDEPT
Keywords:
Comments:
Creation Date: 10/12/2011 2:29 AM
Change Number: 2
Last Saved On: 10/12/2011 2:29 AM
Last Saved By: admin
Total Editing Time: 1 Minute
Last Printed On: 10/12/2011 2:29 AM
As of Last Complete Printing
Number of Pages: 5
Number of Words: 791 (approx.)
Number of Characters: 4,511 (approx.)