



**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
QUESTION BANK**

SUB CODE / SUBJECT: CS1202/COMPUTER ARCHITECHTURE

YEAR / SEM: II / III

**UNIT I
BASIC STRUCTURE OF COMPUTER
PART – A (2 MARKS)**

1. What is meant by the stored program concept?
2. What are the basic functional units of a computer?
3. What is the use of buffer register?
4. Define memory access time.
5. Write the differences between RISC and CISC.
6. What is meant by MAR and MDR?
7. What is an interrupt?
8. Why data bus is bidirectional in most microprocessors?
9. What do you mean by multiprogramming or multitasking?
10. Give the basic performance equation.
11. What are the limitations of assembly language?
12. What are the two techniques used to increase the clock rate R?
13. What are big-endian and little-endian representations?
14. What is the information conveyed by addressing modes?
15. What are the different types of addressing modes available?
16. What is indirect addressing mode?
17. What is indexed addressing mode?
18. Define auto increment mode of addressing?
19. Define auto decrement mode of addressing?
20. What are condition code flags?
21. What is the use of assembler directive?
22. What is meant by straight – line sequencing?
23. What is stack?
24. Which data structure is best supported using indirect addressing mode?
25. What are the differences between Stack and Queue?

PART - B

1. Explain the basic functional units of a simple computer. (16)
2. Explain the basic I/O operations of modern processors. (16)
3. Explain various addressing modes found in modern processors (16)
4. (a) Explain various assembler directives used in assembly language program (08)
(b) Discuss various issues to be considered while assigning the ISA of a processor (08)
5. (a) What are stack and queues? Explain its use and give its differences (10)
(b) Write an assembly language to find the biggest number among given three numbers (6)

UNIT II
ARITHMETIC UNIT
PART – A (2 MARKS)

1. Draw the full adder circuit using two half adders and give the truth table.
2. Why floating point number is more difficult to represent and process than integer?
3. What are the two approaches used to reduce delay in adders?
4. What is a carry look-ahead adder?
5. Discuss the principle behind the Booth's algorithm?
6. How can we speed up the multiplication process?
7. What is bit pair recoding? Give an example.
8. What are the two methods of achieving the 2's complement?
9. What is the advantage of using Booth algorithm?
10. Write the algorithm for restoring division.
11. Write the algorithm for non restoring division.
12. Define IEEE floating point single and double precision standard.
13. When can you say that a number is normalized?
14. Explain about the special values in floating point numbers.
15. Write the Add/subtract rule for floating point numbers.
16. Write the multiply rule for floating point numbers.
17. What is the purpose of guard bits?
18. What are the ways to truncate the guard bits?
19. Define carry save addition (CSA) process.
20. What are generated and propagate function?
21. What is excess-127 format?
22. What is a ripple carry adder?
23. Draw the structure of 4-bit MSI ALU circuit block.
24. What are the various ways of representing signed integers in the system?
25. Give the booth's recoding and bit pair recoding of the number 100011100100101.

PART – B

1. (a) Discuss the principle of operation of carry-look ahead adders. (08)
(b) Discuss the non-restoring division algorithm. Simulate the same for 23/5. (08)
2. (a) Multiply the following pair of signed 2's complements numbers using bit pair recoded multiplier: Multiplicand = 110011 Multiplier = 101100. (08)
(b) Describe the algorithm for integer division with suitable example. (08)
3. With a neat sketch, Explain in detail about logic design for fast adders. (16)
4. Describe how the floating-point numbers are represented and used in digital arithmetic operations. Give an example. (16)
5. (a) Explain the representations of floating point numbers in detail. (06)
(b) Give the block diagram of the hardware implementation of addition and subtraction of signed number and explain its operations. (10)
6. (a) Design a multiplier that multiplies two 4-bit numbers. (06)
(b) Explain the working of floating point adder and subtractor. (10)

UNIT III

BASIC PROCESSING UNIT

PART – A (2 MARKS)

1. What are the limitations of super scalar device?
2. Define pipeline speedup.
3. What is a processor clock?
4. Write down the control sequence for Move (R1), R2.
5. What is the function of a TLB (translation look-aside buffer)?
6. What is the WMFC step needed when reading from or writing to the main memory?
7. Define register file.
8. Define the hardware organization of two-stage pipeline?
9. What is the role of cache memory in pipeline?
10. Name the methods for generating the control signals.
11. Define hardwired control.
12. Discuss the principle of operation of a micro programmed control.
13. Differentiate micro programmed control from hardwired control.
14. Define parallelism in microinstruction.
15. What are the types of microinstructions available?
16. Differentiate horizontal microinstruction from vertical microinstruction.
17. What is MFC?
18. What are the major characteristics of a pipeline?
19. What is a pipeline hazard?
20. What is data hazard?
21. What is instruction or control hazard?
22. Define structural hazards.
23. What is side effect?
24. What do you mean by branch penalty?
25. What is branch folding?
26. What do you mean by delayed branching?
27. What are the two types of branch prediction techniques available?
28. What is the ideal speedup expected in a pipelined architecture with n stages. Justify your answer.
29. Draw the structure of two stage instruction pipeline.

PART – B

1. Give the organization of typical hardwired control unit and explain the functions performed by the various blocks. (16)
2. Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. (16)
3. Explain in detail about instruction execution characteristics. (16)
4. With a neat block diagram, explain in detail about micro programmed control unit and explain its operations. (16)
5. (a) Explain the execution of an instruction with diagram. (08)
(b) Explain the multiple bus organization in detail. (08)
7. (a) Explain the function of a six segment pipeline showing the time it takes to process eight tasks. (10)
(b) Highlight the solutions of instruction hazards. (06)
9. (a) Explain the instruction cycle highlighting the sub-cycles and sequence of steps to be followed. (08)
(b) Illustrate memory read and write operation. (08)

UNIT IV
MEMORY SYSTEM

PART – A (2 MARKS)

1. Define Memory Access time for a computer system with two levels of caches.
2. How to construct an $8M * 32$ memory using $512 K * 8$ memory chips.
3. Write two advantages of MOS device.
4. List the factors that determine the storage device performance.
5. What will be the width of address and data buses for a $512K * 8$ memory chip?
6. Define memory cycle time.
7. What is RAM?
8. What is cache memory?
9. Explain virtual memory.
10. List the various semiconductors RAMs?
11. What do you mean by static memories?
12. Define DRAM's.
13. Define DDR SDRAM.
14. What is ROM?
15. What is the mapping procedures adopted in the organization of a cache Memory?
16. Give the format for main memory address using direct mapping function for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.
17. Give the format for main memory address using associative mapping function for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.
18. Give the format for main memory address using set associative mapping function for 4096 blocks in main memory and 128 blocks in cache with 16 blocks per cache.
19. Define Hit and Miss rate?
20. What are the enhancements used in the memory management?
21. What is meant by memory management unit?
22. What is meant by memory interleaving?
23. What do you mean by seek time?
24. What is disk controller?
25. What is RAID?
26. Define data stripping?
27. How the data is organized in the disk?
28. Define latency time.
29. What is the significance of TLB?

PART – B

1. (a) Discuss the various mapping techniques used in cache memories. (08)
(b) A computer system has a main memory consisting of 16 M words. It also has a 32Kword cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.
 - Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format.
 - How will the main memory address look like for a fully associative mapped cache? (08)
2. (a) Explain the concept of virtual memory with any one virtual memory management technique. (08)

CS1202 COMPUTER ARCHITECTURE

- (b) Give the basic cell of an associative memory and explain its operation. Show how associative memories can be constructed using this basic cell. (08)
3. Give the structure of semiconductor RAM memories. Explain the read and write operations in detail. (16)
4. (a) Explain the organization of magnetic disks in detail. (08)
(b) Write a short notes on PCI (08)
5. (a) A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the caches accommodate? (10)
(b) Explain the concept of memory hierarchy. (06)

UNIT V

I/O ORGANIZATION

PART – A (2 MARKS)

1. What are the functions of I/O interface?
2. How does the processor handle an interrupt request?
3. What are the necessary operations needed to start an I/O operation using DMA?
4. What are the three types of channel usually found in large computers?
5. Why does a DMA have priority over the CPU when both request a memory transfer?
6. What is the advantage of using interrupt initiated data transfer?
7. Why do you need DMA?
8. What is the difference between subroutine and interrupt service routine?
9. What is the need for interrupt masks?
10. How does bus arbitration typically works?
11. How does a processor handle an interrupt?
12. Distinguish synchronous bus and asynchronous bus.
13. Why I/O devices cannot be directly be connected to the system bus?
14. What are the major functions of I/O system?
15. What is an I/O interface?
16. Write the factors considered in designing an I/O subsystem?
17. Explain Direct Memory Access.
18. Define DMA controller.
19. What is polling?
20. What is the need of Interrupt controller?
21. What is a priority interrupt?
22. Define bus.
23. Define synchronous bus.
24. Define asynchronous bus.
25. State the differences between memory mapped I/O and I/O mapped I/O.
26. Define interrupt.
27. Define exception.
28. What are the different methods used for handling the situation when multiple interrupts occurs?
29. What is a privileged instruction?
30. What is bus arbitration?
31. What is port? What are the types of port available?
32. What is a parallel port?
33. What is a serial port?
34. What is PCI bus?

35. What is SCSI?
36. Define USB.

PART – B

1. Explain the functions to be performed by a typical I/O interface with a typical input output interface. (16)
2. (a)Discuss the DMA driven data transfer technique. (08)
(b)Discuss the operation of any two input devices (08)
3. Explain in detail about interrupt handling. (16)
4. Explain in detail about standard I/O interface. (16)
5. Describe the functions of SCSI with a neat diagram. (16)
6. (a)What is the importance of I/O interface? Compare the features of SCSI and PCI interfaces.(08)
(b) Explain the use of vectored interrupts in processes. Why is priority handling desired in interrupt controllers? How does the different priority scheme work? (08)
7. Write note on the following.
 - Bus arbitration
 - Printer process communication
 - USB
 - DMA (16)