



KINGS

COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2008-2009 / ODD SEMESTER

QUESTION BANK

SUBJECT CODE : EC 1202

SEM / YEAR : III / II

SUBJECT NAME : DIGITAL SYSTEM DESIGN

UNIT – 1

BASIC CONCEPTS AND COMBINATIONAL CIRCUITS

PART – A (2 Marks)

1. What is duality theorem?
2. What do you meant by Excess – 3 code?
3. What is gray code? What are its applications?
4. Convert $(268.75)_{10}$ to Octal & Hexadecimal?
5. State Demorgan's Law?
6. Perform 2's complement subtraction of $010110 - 100101$.
7. Plot the expression on k-map.

$$1) F(W,X,Y) = \sum m(0,1,3,5,6) + d(2,4)$$

8. State the principle of Duality?
- 9.

PART - B

1. (a) Illustrate the following codes with an example (minimum 2 examples)
 1. Excess –3 code (3)
 2. BCD code (3)
 3. Gray code (6)
- (b) Convert the following Hexadecimal numbers to decimal

(a)1CH	(b)A85H	(c) E5H	(d) B2F8H	(4)
--------	---------	---------	-----------	-----
2. a. Explain Boolean laws & rules in detail? (8)

- b. (i) Define minterm & maxterm with example (4)
 (ii) Minimize the expression (4)

$$Y = ABC + ABC + ABC + ABC + ABC$$
3. a. Reduce the following function using K-map technique?
 (i) $f(A,B,C,D) = \pi M(0,2,3,8,9,12,13,15)$ (4)
 (ii) $f(W,X,Y,Z) = \Sigma m(0,3,4,7,9,12,14)$ (4)
- b. What are don't care conditions? Reduce the following function using K-map technique. $F(A,B,C,D) = \pi M(0,3,4,7,8,10,12,14) + d(2,6)$ (8)
4. a. Explain the procedure for converting binary to gray code number and gray code to binary number with example (8)
- b. Minimize the following using karnaugh map. Implement the resultant functions using NOR gates only.
 $f(A,B,C,D,E) = \pi M(2,4,7,9,26,28,29,31)$ (8)
5. a. Design a 4-bit parallel adder using full adders (8)
 b. Explain about Look ahead carry generator (8)

UNIT – 2

SEQUENTIAL CIRCUITS

PART – A (2 Marks)

1. Define half adder & full adder?
2. What do you mean by encoder?
3. Write a short note on parity generator?
4. Define the terms fan-in & fan out?
5. What are universal gates?
6. Write short notes on edge triggered flip-flop?
7. How synchronous counters differ from asynchronous counter?
8. What is JK flip-flop?
9. List the basic types of Shift Registers in terms of data movement?
10. Write short notes on PRBS generator?

PART - B

1. Draw a tristate TTL gate and explain its operation? (16)
2. a. Draw and explain the block diagram of PLA. (8)
 - b. Draw the symbol truth table & the equation of the
 1. Basic gates (4)
 2. Universal gates (4)
3. Explain in detail (1) comparator (2) encoder (3) decoder (16)
4. a. Give the comparison between
 1. Combinational circuits & Sequential circuits (4)
 2. Synchronous sequential circuits & Asynchronous Sequential circuits (4)
 - b. Convert
 1. SR-flip-flop into JK flip –flop (4)
 2. JK – flip-flop into T flip-flop (4)
5. a. Draw & explain the block diagram of Moore & Mealy model? (8)
 - b. Explain the operation of
 1. 4 bit Serial –in- serial-out Shift Register (4)
 2. 4-bit Serial-in-parallel – out Shift register (4)

UNIT – 3**FUNDAMENTAL MODE SEQUENTIAL CIRCUITS****PART – A (2 Marks)**

1. What are hazards?
2. What are races & cycles?
3. Define critical race & non critical race?
4. Define state assignment?
5. Write a note on stable state & unstable state?
6. What is a race?
7. What is an asynchronous sequential circuit?
8. Define cycle?
9. What is the cause for essential hazard?
10. Define static hazard?

11. When do hazards occur?
12. What are the techniques used for making a critical race free-state assignment.
13. Define shared row state assignment?
14. Define one hot state assignment?
15. Define fundamental mode sequential circuit and pulse mode sequential circuit?

PART - B

1. a. Explain the procedure to give hazard – free realization of a BOOLEAN FUNCTION. **(8)**
 - b. Explain Static, dynamic & essential hazards in digital circuit. Give hazard – free realization for the following Boolean function **(8)**

$$f(A,B,C,D) = \Sigma m(2,3,5,7,10,14)$$
2. a. Write short notes on
 1. Shared row state assignment **(4)**
 2. one-hot state assignment **(4)**
- b. What are the steps for:
 1. Analysis of asynchronous sequential circuit? **(4)**
 2. Design of asynchronous sequential circuit? **(4)**
3. a. List the different technique used for state assignment? **(8)**
 - b. Write notes on the following giving one example for each.
 1. Stable state **(2)**
 2. Unstable state **(2)**
 3. Cycles **(2)**
 4. Race **(2)**
4. Design an asynchronous sequential circuit with two inputs X & Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change in X. Use SR latch for implementing the circuit. **(16)**
5. Obtain the primitive flow table for an asynchronous circuit that has two inputs x,y and one output z. An output z=1 is to occur only during the input state xy=01 and then if the input state xy=01 is preceded by the input sequence

$$xy=01,00,10,00,10,00.$$
 (16)
6. a. Describe the hazards that could occur in asynchronous sequential circuits.

What are the ways in which they get eliminated? **(8)**

 - b. Design a circuit with primary inputs A and b to give an output Z equal to 1 when

A becomes 1 if B is already 1. Once $Z=1$ it will remain so until A goes to 0.

Draw waveform diagram, total state diagram, primitive flow table for designing this circuit. (8)

7. a. Draw the fundamental mode asynchronous circuit and explain in detail. (8)

b. Illustrate pulse mode asynchronous circuit. (8)

UNIT – 4

MEMORY, CPLDs AND FPGAs

PART – A (2 Marks)

1. Give the Block diagram of Memory unit.
2. Give the classification of semiconductor memories
3. Explain the organization of RAM with the help of neat diagram.
4. Give the steps for memory Read operation & write operation
5. What are two types of RAM
6. Define static RAM & give the types
7. Define Dynamic RAM & Dynamic RAM.
8. Compare static RAM & Dynamic RAM
9. What is refreshing & how it is done
10. Draw the timing diagram for READ cycle
11. Draw the timing diagram for WRITE cycle
12. Design 16K X8 RAM using two 4KX8 ICs
13. What is PROM?
14. What is EPROM?
15. What is EEPROM?
16. What are the classifications of Programmable Logic Device?
17. Define field & array.
18. What do you mean by configurable logic blocks CLBs?
19. Draw the general FPGA chip architecture.
20. Draw the Xilinx 3000 series configurable logic block.
21. Draw the I/O block of Xilinx FPGA.
22. Illustrate the concept of 16 X 8 bit ROM arrangement with diagram

23. Explain the basic structure of a 256 X 4 static RAM with diagram.
24. What do you mean by ASIC?
25. What is ROM?
26. What is PLA?
27. What is PAL?

PART - B

1. (i) Describe the typical ROM internal organization with necessary diagram (8)
 (ii) Illustrate the concept of 16X 8 bit ROM arrangement with diagram (8)
2. i) Explain the basic structure of a 256 X 4 static RAM with neat diagram (8)
 ii) Write a note on
 - (1) MOSFET RAM cell (4)
 - (2) Dynamic RAM cell (4)
3. i) Draw a dynamic RAM cell & explain its operation (8)
 ii) Explain in detail
 1. Memory decoding (4)
 2. EEPROM (4)
4. i) Write short notes on (8)
 1. RAM
 2. Types of ROM's
 ii). Implement the following two Boolean functions with a PLA (8)

$$F_1(A,B,C) = \Sigma(0,1,2,4) \qquad F_2(A,B,C) = \Sigma(0,5,6,7)$$
5. Explain how PROM can be useful for combinational logic design. Discuss how PAL improves this design process. (16)
6. What are the different classifications of memory? Explain in detail about types and applications of ROM. (16)
7. (i) Mention the steps involved in the design of a digital combinational circuits with an example (6)
 (ii) Using the simplified connection format of PLA, show how an 8 X 1 PROM could be programmed to implement the logic function $F = \Sigma(1,4,5,7)$ (10)
8. i) Draw the block diagram of a PLA device & briefly explain each block. (8)
 ii) Explain the Organization of RAM with the help of neat diagram (8)
9. i) Design a 16 bit ROM array and explain and explain the operation (8)

- (ii) Write short notes on FPGA (8)
- 10.i) Define static RAM and explain its classification. (8)
- ii) Explain the working of dynamic RAM cell. (8)
11. i) Write short notes on: PROM, EPROM & EEPROM. (8)
- ii) Write a short note on memory decoding (8)
12. Explain the general architecture of FPGA. (16)
13. Explain XC4000 architecture. (16)

UNIT - 5

LOGIC FAMILIES

PART – A (2 Marks)

1. What are the two types of logic levels used?
2. Define the following parameters?
 - a. Current & Voltage
 - b. Fan Out & Fan In
 - c. Noise Margin
 - d. Propagation delay
 - e. Power dissipation
 - f. Speed Power Product
3. Draw the circuit diagram & explain the operation of 2 i/p TIL NAND gate with totem-pole O/P.
4. Write a note on Multiple emitter transistor
5. For a certain IC family, Propagation delay is 10ns with an average power dissipation of 6mw. What is its speed power product?
6. A two i/p NAND gate has $V_{CC} = +5V$ and $1K\Omega$ load connected to its output. Calculate the output voltage. a) When both input are low b) When both input are high
7. Describe the difference between current sinking & current sourcing.
8. State advantages & disadvantages of totem pole output.
9. Describe the characteristic of TTL family
10. Compare totem pole and open collector output?
11. Draw the circuit diagram and explain the operation of 2 input TTL NAND gate with open collector output
12. Draw the circuit diagram of CMOS inverter.
13. What are the points to be considered while interfacing two circuits or systems?

14. Compare CMOS and TTL families.
15. Find the optimum value of the pull-up resistor of a TTL open collector inverter for a fan out of 5.
16. Find maximum number of tri-state inverters can be connected to a common bus bar, when output of the inverter is high. The common bus bar is driving 5 TTL ICs.
17. Give the comparison between TTL, CMOS, ECL
18. Explain the wired-AND connection?
19. Explain output switching times using waveforms?
20. Define rise time and fall time?
21. What are the advantages of digital Integrated circuits?
22. What is Bi-CMOS logic?
23. Give the advantages and disadvantages of Bi-CMOS logic?
24. Design a CMOS transistor circuit that has the functional behavior

$$Z = [A.(B+C)]'$$
25. What are the sources of stray capacitance in the logic circuit?

PART - B

1. i) Draw the CMOS NAND gate and explain its operation. What are the characteristics of CMOS? (10)
 ii) Draw a tri-state TTL gate and explain its operation (6)
2. Explain the wired-AND connection (16)
3. i) Compare the totem-pole and open-collector outputs (8)
 ii) Draw and explain the basic CMOS Inverter circuit. (8)
4. i) Draw and explain the circuit of 2 input CMOS NOR gate (8)
 ii) Discuss the characteristics of CMOS family (8)
5. Explain with neat diagram interfacing of a TTL gate deriving CMOS gates and vice versa. (16)
